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Design of inherently wide-band microwave frequency doubler and tripler in microstrip

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ABSTRACT (UNCLASSIFIED)

Two modern wide-band and frequency agile radar systems, currently under construction at TNO-FEL, require the development of a wide-band S-band frequency doubler and a wide-band X-band frequency tripler. The wide-band requirement, however, is hard to meet when using the classical approach. Wave-form invariance as an alternative concept to achieve inherently wide-band behaviour is proposed. From this, a new design goal is derived and formulated: constant admittance at the terminals of the non-linear device within each harmonic sub-band. A frequency doubler has been designed and built based on this concept; the conversion efficiency measures (1.0 ± 0.7) dB in the 2.8 ... 3.6 GHz design band. Also, a frequency tripler has been designed and built based on this concept; the conversion efficiency measures (-10.4 ± 0.6) dB in the 8.5 ... 10.5 GHz design band. Both examples prove the validity and practical suitability of this alternative concept.

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titel	:	Ontwerp van inherent breedbandige microgolf frequentie-verdubbelaar en -verdrievoudiger in microstrip
auteur(s)	:	Ir. J.C. Henkus
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SAMENVATTING (ONGERUBRICEERD)

Twee moderne breedband en frequentie hoppende radarsystemen, momenteel in aanbouw bij TNO-FEL, vereisen de ontwikkeling van een breedband S-band frequentie-verdubbelaar en een breedband X-band frequentie-verdrievoudiger. De breedband eis is echter moeilijk te vervullen bij gebruik van de klassieke benadering. Golfvorm-invariantie als alternatief concept voor het bereiken van inherent breedband gedrag is voorgesteld. Hier vanuit is een nieuw ontwerpdoel afgeleid en geformuleerd: constante admittantie op de aansluitingen van de niet-lineaire component binnen elke harmonische subband. Een frequentie-verdubbelaar is ontworpen en gebouwd gebaseerd op dit concept; de conversie-efficiëntie meet (1.0 ± 0.7) dB over de 2.8 ... 3.6 GHz ontwerpband. Ook is een frequentieverdrievoudiger ontworpen en gebouwd gebaseerd op dit concept; de conversie-efficiëntie meet (-10.4 ± 0.6) dB over de 8.5 ... 10.5 GHz ontwerpband. Beide voorbeelden bewijzen de geldigheid en praktische bruikbaarheid van dit alternatieve concept.

INTRODUCTION

Modern radar systems require wide-band agile transmitters. At the TNO Physics and Electronics Laboratory, two of such advanced radar systems are under construction and will operate in S-band (FELSTAR/SMRA) and X-band (MIRA), both requiring 20% or more relative instantaneous band-width. The Laboratory has already developed an agile L-band synthesizer. Therefore, a frequency doubler (L- to S-band) and tripler (S- to X-band) become mandatory. However, microwave frequency triplers, in particular with respect to wide-band performance, are not or not sufficiently addressed in literature and are evidently not commercially available. Unfortunately, it is tedious and difficult to design frequency multipliers that possess acceptable wide-band behaviour.

Due to the relative large time-constant involved, the potential use of Automatic-Gain-Control as a repressive means to cope with fluctuating output power is not acceptable in this case of extreme pulse-to-pulse frequency agility.

The first aim of this report and the underlying investigations is to search for or to establish a straightforward and generic design procedure for microwave frequency multipliers which inherently solves the wide-band problem.

The second aim is to actually deliver a frequency doubler and tripler suitable for implementation in FELSTAR/SMRA and MIRA.

This report has been written for the reader equipped with a general theoretical background of networking and microwaves but lacking specific reference in microwave frequency multipliers.

[1] is devoted to the TNO-FEL agile synthesizer. One of its paragraphs treats the frequency doubler design. This frequency doubler, however, is an aggregated result of the present study as reported here.

During the course of the present study, the need for diplexers was recognized. Since the design of diplexers can be autonomously dealt with, it was decided to publish the formulated diplexer design procedure in a separate report ([2]).

P.J. Koomen has participated in initial brainstorming and factfinding discussions.

B.C.B. Vermeulen has designed, according to [2], the tripler's input-diplexer and has also performed many of the measurements.

Chapter 1 describes classical frequency multipliers and formulates the proposed alternative design concept. Chapter 2 outlines the design of a frequency doubler based on this concept. Chapter 3 outlines the design of a frequency tripler based on this concept. Conclusions and recommendations are formulated in chapter 4. Appendices A, B, E, and F present the measured conversion efficiency and harmonic components of the frequency doubler and tripler, respectively. Appendices C and D present the measured reflection coefficients and transfer functions of the input- and output-diplexer.

1 DESCRIPTION OF CLASSICAL FREQUENCY MULTIPLIERS AND A PROPOSED ALTERNATIVE DESIGN CONCEPT FOR INHERENTLY WIDE-BAND FREQUENCY MULTIPLIERS

1.1 Description of classical frequency multipliers

The function of a frequency multiplier is to convert a singular sinusoidal input-signal with frequency f_i into a singular sinusoidal output-signal with frequency n f_i with 'n', a positive integer.

Classically, this is realized by applying the input-signal to a two-terminal non-lineair device. This device reshapes the incident sinusoidal signal to another periodic non-sine-shaped signal in the time-domain, thereby introducing harmonic spectral components as follows from Fourier-expansion. Non-linearities of the even-type generate only even-order harmonics (n = 0, 2, 4 ...) and in the case of odd-types only odd-order harmonics (n = 1, 3, 5, ...); a combination of both types is also possible. However, only one specific harmonic component is exclusively required at the output of the multiplier. Therefore, a Band-Pass-Filter (BPF) is added between the non-linear device and the multiplier's output to suppress all harmonic components but the desired one. To prevent pulling of the microwave generator due to interaction with the generated harmonic components, a Low-Pass-Filter (LPF) is inserted between the multiplier's input and the non-linear device (in case of even-order non-linearities, the introduced DC-component must be blocked also).

In general, the device-impedances for the fundamental and desired harmonic component lie far from the 50Ω system-impedance resulting in an intolerable small RF → RF power conversion efficiency C_n of the multiplier. Hence, the use of two Matching-Networks (MN) is mandatory. However, all other harmonic components are still present at the terminals of the non-linear device (and will not be suppressed by the filters either) and require adequate effective terminating admittances $Y(\omega) = G(\omega) + j\,B(\omega)$. Optimal conversion efficiency demands, with respect to this admittance, absence of conductivity (G = 0) and a finite susceptance, optimized for each harmonic component that is left. These extra demands can, in theory, be accomplished by extension of the set of frequency-intervals for which the impedance of the MN's is specified, in such a way that these other harmonic frequencies are incorporated as well (the LPF and BPF by which the MN's are 'terminated' must have already been defined).

A block diagram of the classical frequency multiplier as described above is shown in figure 1.

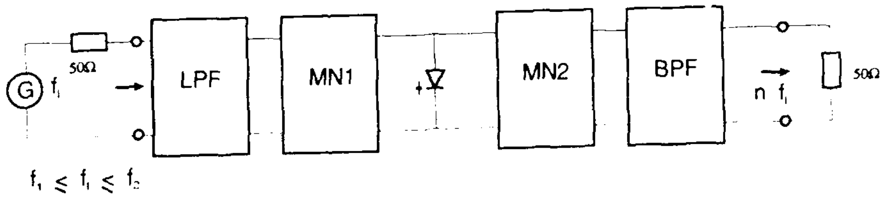

Fig. 1: Block diagram of the classical microwave frequency multiplier. The frequency of the input-signal, f_i, ranges from f_1 to f_2 and is multiplied n-times.

Although the LPF and MN1 have been discussed and drawn as cascaded, separate items, their functions may be combined into one integrated two-port (also MN2 and BPF).

For small values of the frequency multiplication factor 'n', a depletion layer varactor diode is chosen while for large values a Step-Recovery-Diode (SRD) is normally used. Both the varactor and SRD are essentially purely reactive devices (no energy dissipation) and hence allow for potentially for high conversion efficiencies. The use of a pure resistive non-linear device has only been encountered in literature by the author ([14]).

Under the condition of permanent absence of unwanted harmonics and when assuming idealized filters, the relative instantaneous band-width[1] is limited to 70.7% (1 octave, $f_2 = 2\ f_1$) for doublers (but only when odd harmonic components are absent, otherwise 40.8%) and to 51.6% ($f_2 = {}^5/_3\ f_1$) for triplers (but only when even harmonic components are absent, otherwise 28.9%).

Advantages of this type of frequency multipliers are.

1) Reactive non-linear devices allow for *potentially* large RF → RF power conversion efficiencies[2] (C_n up to 70%),
2) Usable well into the submillimeter-frequency region (n f_2 >> 100 GHz),
3) Usable up to high RF-(peak)power levels (at least several Watts in C.W.-mode at 50 GHz),
4) No DC-power required (passive two-terminal non-linear devices).

1) Absolute instantaneous bandwidth relative to the (geometric) central frequency.

2) It is noted that, in contrast to what may be suggested by intuition, large conversion efficiencies by themselves do not improve close-carrier phase-noise characteristics but only contribute positively to the RF-energy/power balance.

Remarks on these advantages in relation to the currently required frequency doubler (n = 2, n f_1 = 2.8 GHz, n f_2 = 3.6 GHz for FELSTAR/SMRA) and tripler (n = 3, n f_1 = 8.5 GHz, n f_2 = 10.5 GHz for MIRA), both with flat output-amplitude over the entire frequency-band (wide-band behaviour):

Re 1, 2, 3, 4) These items are not mandatory for the current application (no extreme high frequency (<= 10 GHz), low power levels (<= 10 mW), DC-power available).

Disadvantages with respect to designability and performance of the classical frequency multiplier are:

1) Both the input and output-branche merge into one central node at which, due to the non-linear device, all harmonic components are present. Hence, there is no inherent isolation between the input and output-branche that could otherwise (partly) avoid unwanted harmonic components from leaking away to source or load. In order to maintain cleanness of the output-spectrum, this lack of isolation must be compensated for by impressing additional stop-band rejection requirements on the external filters.

2) The conversion efficiency from f_i to n f_i depends on the complex admittance Y(ω) by which the non-linear device is shunted at f_i and all of its harmonics; thus, for a maximal conversion efficiency, the admittance has to be optimized at each of those frequencies. This step involves integral[1] and iterative[2] optimization enclosing recurrent analysis of the actual non-linear behaviour and must be repeated for all (or a representative selection of) input-frequencies f_c ranging from f_1 to f_2. Unfortunately, a single non-linear analysis is delicate and time-consuming, even when using modern Harmonic-Balance-Method based software like EEsof's LIBRA, assuming that it actually can cope with optimization schemes of this type. Hence, determination of the complex admittance Y(ω) *optimized* for *all* input frequencies (from f_1 to f_2) and *all* of its associated harmonic frequencies will be an extremely laborious task.

1) The transfer-function can not be factorized into a series of single-parameter sub-functions: hence, integral or simultaneous optimization must be chosen rather than sequential parameter optimization.

2) The transfer-function is known only implicitely (by means of constitutional and specific circuit equations), so an iterative approach is necessary.

3) The design of MN's (suited for implementation in MIC-technology) fulfilling admittance requirements as determined under item 2) is hampered by a fundamental and a practical consideration:
   - Beyond a MN's pass-band, the admittance does not vanish but an almost pure susceptance remains which changes with frequency. Since the MN's are connected in parallel, mutual interaction occurs so the MN's can not be regarded and designed anymore as two independent, separate blocks.
   - The real and imaginary part of the optimal admittance will turn out to be whimsical functions of frequency, in particular due to the wide-band requirements and the many harmonic components involved. This whimsicality imposes use of circuits of complex structure in order to lower residual discrepencies in admittance. Due to this complexity, critical dependance of potential wide-band performance on even small deviations (systematic and random) in circuit implementation must be expected.

4) Relative large RF input power must be available in order to drive the passive non-linear device into a suitable mode of operation ($P_{in} \geq 0.1 \ldots 0.3$ W).

Remarks on these disadvantages in relation to the currently required frequency doubler and tripler:

Re 2) The disadvantage discloses almost exclusively in large relative band-width applications as in the present case. For single-frequency applications the disadvantage may be acceptable. Furthermore, since wide-band performance is then no key-parameter anymore, the optimal admittance need not be known precisely and deviations will become tolerable.

Re 3) The disadvantage is mainly associated with the large relative bandwidth requirement as in the present case. For single-frequency applications simpler MN's will suffice. Moreover, it becomes feasible to rely on emperical circuit tuning in order to obtain almost optimal conversion efficiency; hence, the initial determination of optimal admittance and design of MN's does not *have* to be accurate any longer in the single-frequency case.

In literature, no examples of wide-band classical frequency multipliers were found by the author, other than the second and third reference in [4], namely [12] and [13]. Unfortunately, the latter two appeared not to be (regularly) available at national level.

1.2 A proposed alternative design concept for inherently wide-band frequency multipliers

In summary, in the classical approach the design goal is to maximize conversion efficiency at all possible input-frequencies. The *maximal* conversion efficiency itself is almost independant of frequency. It is just because of this fact that wide-band performance can *potentially* be attained (apart from the associated design and implementation problems).

Proposed is to adapt an alternative concept. In this approach the most important step is to explicitely recognize that the multiplier's performance is completely determined by the non-linear device voltage's time-domain representation, thus wave-*form* and amplitude. When the surrounding circuit inhibits the time-domain representation to change with increasing input-frequency, then the Fourier-expansion remains also unchanged. Hence, alternatively, wide-band performance is acquired.

The process of interaction between the voltage and current wave-forms across and through the non-linear device and the externally applied shunt-admittance is shown in figure 2.

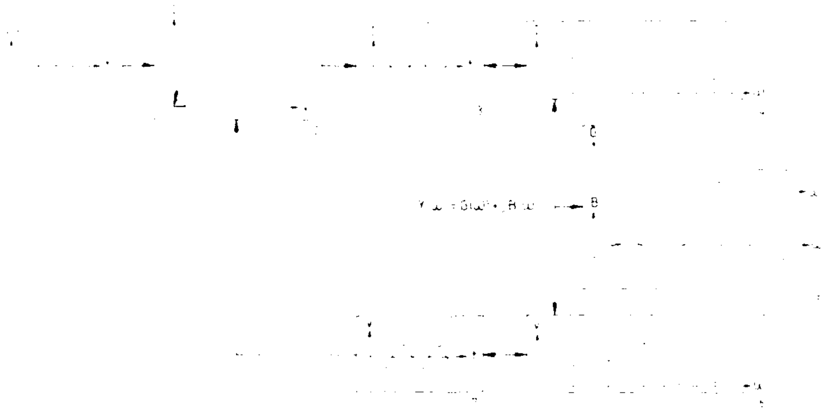

Fig. 2: Process of interaction between wave-forms and admittance. The labels at the right lower-corner will be referred to from the text.

Box 1 shows the sinusoidal signal with frequency f_i that is initially applied to the non-linear device. The non-linearities involved are characterized and shown in box 2: in this case, the

I_{ds}/V_{ds}-relations of a MESFET. These non-linearities introduce harmonic components resulting in a time-domain representation as shown in box 3 and a frequency-domain representation as shown in box 4. Each rectangle in this box as drawn by thin lines is called a harmonic subband and specifies the frequency-interval that will be occupied by the harmonic component (in that rectangle) when the input frequency is swept from f_1 to f_2 (in this case $f_2 = 1.2\, f_1$).
The non-linear device is shunted by an external admittance $Y(\omega)$. Therefore, the Norton-current from the device induces a voltage across the terminals as defined by:

$$V(\omega) = Y^{-1}(\omega) \cdot I(\omega)$$
$$\text{with } Y(\omega) = G(\omega) + j\, B(\omega)$$

as is shown in boxes 5 and 6. Box 7 shows the voltage time-domain representation. In general, when $Y(\omega)$ is not restricted , the current and voltage wave-form differ and respond differently to change in input-frequency.
When the circuit is in equilibrium, the current and voltage wave-forms and the current and voltage relations as imposed by the non-linear device are consistant and meet Kirchhoff's laws. During the course of each cycle of the wave, a closed locus in the I/V-domain is passed through with the DC-bias point somewhere in the centre. If the locus and wave-form do not alter as input-frequency increases, Fourier-expansion and conversion efficiency will not change either so wide-band performance is attained. This invariance can only be established when each harmonic component as present at the terminals of the non-linear device is exposed to some admittance that remains constant for that harmonic components as the input-frequency increases from f_1 to f_2, thus within each harmonic subband. However, for any two different sub-bands the specifically applied admittances are allowed to differ, so:

$$Y(k\omega) = G_k + j\, B_k$$
$$\text{for all } \omega \in [2\pi k f_1, 2\pi k f_2],\ k \in N$$

where 'k' stands for a specific harmonic. This is the new design goal for the surrounding circuits to fulfil the condition of wave-form invariance. As will be shown in the following and in next chapters, the design process for the surrounding circuits is passed relative easy in this case.
In practice, the design goal is reached easiest when, for all frequencies, absence of susceptance (B_k=0 for all k) and a single value for the conductive part (e.g. $G_k = 0.02\ \Omega^{-1}$ thus $R_k = 50\ \Omega$ for

all k) is chosen for: effectively speaking a wide-band 50 Ω termination. Implementation may seem trivial but the LPF and BPF functions still have to be incorporated. In this case of resistive termination, current and voltage wave-forms are congruent and in-phase.

Obviously, when the new design goal is employed, the RF → RF power conversion efficiency will not be maximal anymore due to admittance mismatch.
A varactor or SRD as non-linear device is essentially a pumped pure *reactance* leading to extreme dynamic or parametric associated admittances. Therefore, due to admittance mismatch, the loss in conversion efficiency will be dramatic and untolerable.
Alternatively, as the advantages associated with the use of a varactor or SRD appeared not to be mandatory, a GaAs MESFET can be chosen as (active) non-linear device. The non-linearity in this device is concentrated mainly in the static output I-V characteristics, so all important (trans)-admittances will be essential *conductive*, even under dynamic conditions. Besides, in the microwave frequency region, the conductance of commercially available MESFETs is not extreme (with respect to 50Ω). Hence, the loss in conversion efficieny due to admittance-mismatch when using a MESFET will be far from dramatic and for the intended application will probably prove to be acceptable. Furthermore, the two-port nature of the MESFET establishes inherent input-output isolation.

It is implicitely assumed that the characteristics of the non-linear device itself (equivalent Norton-current-source and admittance) do not exhibit frequency sensitivity. Due to unavoidable parasitic capacitances and inductances the assumption is not met when considered strictly. However, since the values of the capacitances and inductances are small and frequency insensitivity has to be maintained only within the sub-bands rather than within one large frequency band as wide as all sub-bands together, the assumption is met by approximation.

Next chapters focus on design of the surrounding circuits and measurement of a complete frequency doubler (ch. 2) and tripler (ch. 3). The designs are based on the alternative concept as introduced in this paragraph.

2 DESIGN AND MEASUREMENT RESULTS OF A WIDE-BAND FREQUENCY DOUBLER

2.1 Design of a wide-band frequency doubler

For the implementation of a frequency doubler, a circuit topology must be synthesized or identified which allows for:

1) separation of the wanted harmonic component from the unwanted components,
2) fulfilment of the admittance design goal for wide-band behaviour.

Item 1) is realized by applying the concept of balanced or (anti-)symmetrical circuits. Item 2) is adressed by careful analysis of the acquired admittances and, from this, the adaption of possible modifications. Figure 3 shows the circuit configuration as induced from such an analysis.

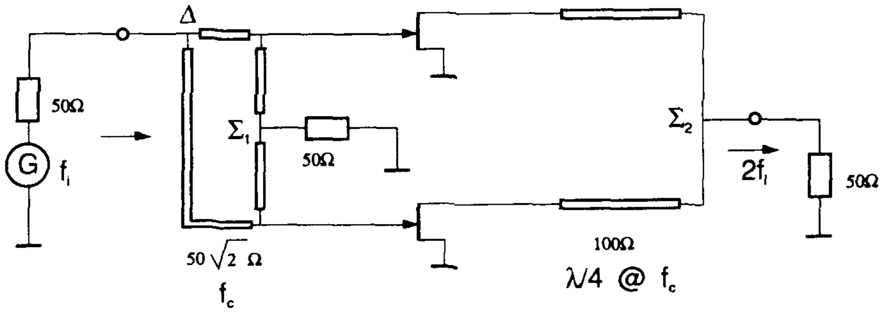

Fig. 3: Frequency doubler circuit topology featuring inherent separation of odd and even harmonic components and wide-band behaviour.

With respect to item 1),analysis of the circuit configuration yields the following:

- Odd harmonic components leaving the drains face a virtual ground at Σ_2 so the output load will not be excited,
- Even harmonic components leaving the drains enter Σ_2 in phase and will add up in the output load,
- Odd harmonic components leaving the gates add up in Δ and will be absorbed in the generator's internal resistance (50 Ω),
- Even harmonic components leaving the gates will be absorbed equally by both the generator's internal resistance and the dummy load at Σ_1.

Since the rat-race between the generator and the two MESFETs maintains phase and amplitude relations fairly well over band-widths up to a large fraction of an octave, the four phenomena hold likewise over such a large band-width. Only the first phenomenon will degrade noticably: at the edges of a 40% wide frequency interval, the suppression of odd harmonic components will be 17dB.

Concludingly:

- Odd harmonic components and 3 dB attenuated even harmonic components enter the generator. Potential interaction, however, can be opposed by insertion of a simple buffer-stage (e.g. MAR-x) for reverse isolation,
- Odd harmonic components (suppressed by 22 dB or better in case of the currently required frequency doubler), the wanted second harmonic component, and higher order even harmonic components of low and decreasing amplitude enter the output load. Depending on ultimate demands on spectral purity, a frequency selective filter can be inserted for extra suppression, although attention to its input match is required (pad or simple buffer-stage for easy match).

With respect to item 2), analysis of the circuit configuration yields the following:

- Odd harmonic components leaving the gates face the generator's internal resistance, thus 50 Ω,
- Even harmonic components leaving the gates face 25 Ω together, thus 50 Ω each,
- Odd harmonic components leaving the drains face, due to a virtual ground at Σ_2, a short-circuited 100 Ω λ/4-stub showing infinite reactance at odd multiples of the central frequency,
- Even harmonic components leaving the drains each face a perfect 100 Ω load which is independant of the phase-length (hence frequency) of the 100 Ω transmission lines.

Since the rat-race maintains a 50 Ω match fairly well over band-widths up to a large fraction of an octave, the first two phenomena hold likewise over such a large band-width.
The third phenomena -infinite reactance for odd harmonic components leaving the drain- holds only at odd multiples of the central frequency; for other frequencies, reactance follows from the 'tan ($^{\pi}/_{2}$ f_i / f_c)'-law which is far from frequency insensitive.
The fourth phenomenon -100 Ω resistance for every even harmonic component leaving the drains- is exactly valid for all frequencies.

Concludingly:

- The admittance design goal for wide-band behaviour is met for both odd and even harmonic components leaving the gates, as well as for even harmonic components leaving the drains.
- Odd harmonic components leaving the drains face frequency sensitive admittances. In practice, this externally applied reactance is shunted by a more or less smoothly sloped drain conductivity from the MESFET's interior.

  Frequency insensitivity can be improved by shunting the two drains by means of one interconnecting:
  - resistor (R) in series with a $\lambda/2$ transmission line (twice $\lambda/4$) of any characteristic impedance,
  - resistor (R) in series with a transmission line (or two halves) of any phase-length, including zero, with R/2 as characteristic impedance.

  However, the MESFET is driven into its non-linear region mainly due to a large voltage swing at the drain terminal from the fundamental (= odd) harmonic component. Therefore, extra shunt conductively is bounded to a maximum such that, given the equivalent Norton current source, the accompanying voltage swing is maintained at an acceptable level. In the current design no extra shunt admittance has been applied.

  Concludingly, the chosen output topology is, when considered strictly, on bad terms with the admittance design goal, but only for odd harmonic components which leave the drains.

A literature search has been performed and the resulting computer listing is available from the author. With respect to (wide-band) frequency doublers the following articles are found to be illustrative.

[3] describes a frequency doubler using a single MESFET, two undefined matching networks and an undefined output filter. The reported measurements indicate -1 dB conversion efficiency, 22% band-width, and high rejection of unwanted harmonic components. All this implies that the matching networks and filter must have had a high order.

Hence, considering the disadvantages discussed in paragraph 1.1, the quality of the doubler that was actually built and measured as design example for generic purposes is questioned.

[4] describes a frequency doubler with two biased SRDs in a balanced topology, both to some degree matched by one $\lambda/4$ transformer. The reported measurements indicate 18% band-width. It is claimed that this large band-width for a SRD frequency multiplier is due to the absence of a

tuned output network which, in its own turn, is allowed by the balance concept. Although not specified in the paper, the required input power is estimated to be 0.1 ... 0.3 W.

[5] describes a frequency doubler using two dual-gate MESFETs in a balance topology, both matched at the gate as well as at the drain, and a coplanar waveguide as balun. The reported measurements indicate a peaked transfer-function with -3 dB band-width in the order of 15% and +12 dB peak conversion efficiency when not driven into compression. The large value of the latter is due to the high gain of cascode-stages like the dual-gate MESFET.
The article describes also a single FET active 180°-phase-shifter/splitter in MMIC as alternative balun: phase-error of not more than 5° is maintained over a 2-12 GHz band.

[6] describes a frequency doubler using two standard gain blocks, two (quadrature) 90°-phase-shifter/splitter/combiner, and a succeeding output-amplifier. The reported measurements indicate an overall (!) conversion efficiency smoothly increasing from -6 dB to -1 dB over one octave and a fundamental frequency rejection of 8.5 dB (mid-band) or better.
It is claimed that all odd harmonic components will be suppressed. However, phase-shift *in front* of and behind the non-linear device has been treated equally but is not allowed due to change in frequency. When the latter effect is recognized, analysis shows that the fundamental component will be suppressed (as claimed), the second harmonic component will loose 3 dB (due to absorption in a dummy load; this partly explaines the extreme small conversion efficiency), and the third harmonic component will pass the output freely (partly in the pass-band). Furthermore, the generator will face inherently impedance match at the fundamental frequency due to the input 90°-hybrid. This feature may be adapted in future designs of frequency multipliers.

[7] descibes a frequency doubler using four Schottky diodes in quad-structure as rectifier and baluns at input and output. The baluns have been implemented by means of microstrip as well as coplanar transmission lines at both sides of a substrate which is mounted in a two-compartment metal box. The lay-out has been emperically optimized. The reported measurements indicate a conversion efficiency between -12 dB and -9 dB and a fundamental frequency rejection of 12 dB or better over one octave at 0.1 W input power.
The use of a diode-quad as presented in this article is well-known for input frequencies less than 1 GHz where it becomes feasible for baluns to be implemented by means of coupled-oil transformers (e.g. Mini-Circuits) thus allowing *multi*-octave performance.

For future designs of frequency doublers [7] is worthwhile to be reconsidered when mechanical issues can be solved and emperical redesigns are allowed.

[8] describes a balanced frequency doubler using two diodes, coaxial stubs and transmission lines, and a balun/stub combination, all implemented by means of up to three concentric hollow metal pipes and a central conductor, thereby constituting coaxial transmission lines. The complete structure forms two halves of a low-pass filter prototype (one half for the input, the other for the output), electrically connected through the diodes. In the design-phase it is assumed that, among others, the diodes can be regarded as a two-port resistance inverter with constant and real parameter K coupling together resistances at two different frequencies (f_i and $2f_i$; other frequencies are ignored) and that the inverter function also holds for reactive impedances that will be present at off-resonance operation in wide-band applications. The reported measurements indicate a conversion efficiency around -3 dB and a fundamental frequency rejection of 15 dB or better over one octave at 0.1 W input power. Such a large conversion efficiency over one octave for a passive frequency multiplier is a surprisingly good result. However, in literature no examples based on [8] were encountered by the author. Nevertheless, for future design of frequency multipliers, [8] is worthwhile to be reconsidered when mechanical issues can be solved. With respect to this, it is specifically recommended to investigate suitability of the coplanar balun of [7] as substitute for the laborious concentric coaxial balun/stub combination.

[15] describes a balanced frequency doubler using two pairs of Schottky diodes and tapered, double-sided bilateral stripline and finline transmission lines. These lines act as baluns with wide-band resistance transforming properties for partial power-match to the diodes. The reported measurements indicate -14.5 dB conversion efficiency at 0.4 W input power, octave band-width in a 3 dB range, and 30 dB fundamental and third harmonic component rejection. When compared to $\lambda/4$-baluns, wide-band behaviour is clearly improved by tapering the constituting transmission lines. However, mechanical drawbacks remain present.

Concludingly:

- The use of a balanced topology in frequency doublers is virtually standard,
- The concept of wave-form invariance in the time-domain and the consequent general design goal as derived in paragraph 1.2 as alternative starting-point to achieve wide-band performance has not been encountered in literature by the author.

The frequency doubler circuit topology as shown in figure 3 remains unmodified and is directly implemented into microstrip technology. A photograph of the implementation is shown in figure 4.

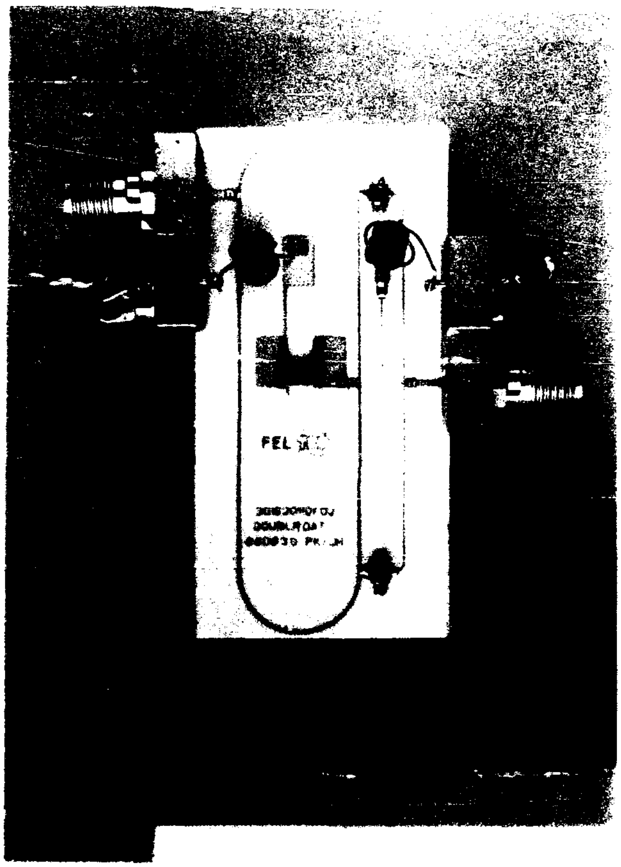

Fig. 4: Photograph of experimental wide-band frequency doubler (L-band to S-band). The design is mainly based on the concept of wave-form invariance to achieve wide-band performance. The rat-race, the two MESFETs, and the two 100 Ω output transmission lines can clearly be identified after comparison with figure 2. The components within the rat-race ring bias and protect the gates. The short $\lambda/4$ stub connected to the output-node injects the externally applied DC-voltage to the drains. The black ferrite beads act as chokes in series with the DC-wires.

The two MESFETs are of the small-signal type and have been selected for appropriate DC-match so that both MESFETs have equal effective bias to achieve the desired balanced mode of operation.

The $\lambda/4$-stub at the output-node unfortunately exhibits a reactance strongly depending on frequency: infinite reactance at odd multiples of twice the central input frequency (k= 2, 6, 10, ...), a large but limited reactance ($\approx + 100\,j\,\Omega$) at odd multiples of the central input frequency (k= 1, 3, 5, ...), and zero reactance at even multiples of twice the central input frequency (k= 4, 8, 12, ...). However, since odd harmonic components (k= 1, 3, 5, ...) are absent, the limited reactance can not change the wave-form and is not of concern. Hence, only for k= 4, 8, 12, ... a major influence from the $\lambda/4$-stub remains. Clearly, the admittance design goal is not entirely met for the latter values of k. For future designs of frequency multipliers it is recommended to investigate modifications of, or alternatives for the $\lambda/4$-stub, e.g. resistive loading of the stub or replacement by an inductive coil with high resonance frequency.

2.2 Measurement results of a wide-band frequency doubler

The frequency doubler as described in this chapter and presented in figure 4 has been subjected to measurement of conversion efficiency and strength of unwanted harmonic components at the output port.

The measurements have been performed by means of a microwave frequency synthesizer and a semi-digital microwave frequency spectrum analyzer. The post-processing function has been used to normalize for the actual frequency response of both the synthesizer and spectrum analyzer.

The conversion efficiency is shown in appendix A: Frequency doubler conversion efficiency (note the 1 dB per division scale). It turns out to be (1.0 ± 0.7) dB over the 2.8 ... 3.6 GHz design band at 8 dBm drive, 3 V drain voltage and 100 mA drain current. Actually, a response of almost one octave (2 ... 4 GHz) has been achieved but, due to necessary band-switching in the spectrum analyzer and the prime focus on the design band, a single interval representation is not given.

The absolute power levels of the first four harmonic components are shown in appendix B: Frequency doubler harmonic components. The suppression of unwanted harmonic components with respect to the second one ranges from -45 ... -12 dBc.

Concludingly, the current frequency doubler does exhibit the anticipated wide-band response and moderate spectral purity.

3 DESIGN AND MEASUREMENT RESULTS OF A WIDE-BAND FREQUENCY TRIPLER

3.1 Design of a wide-band frequency tripler

For implementation of a frequency tripler, a circuit topology must be synthesized or identified which allows for:

1) separation of the wanted harmonic component from the unwanted components,
2) fulfilment of the admittance design goal for wide-band behaviour.

Item 1) is realized by inserting an appropriate low-pass filter (LPF) in the input chain and a band-pass filter (BPF) in the output chain. Item 2) is realized by extention of the filters by means of two one-port shunt-networks that compensate for the admittance of the LPF and BPF in such a way that a 50 Ω resistance is established effectively for all frequencies. These one-ports may be built up from a no-loss two-port network having the second port terminated by an 50 Ω dummy load. In effect, two diplexers are created with the common junctions connected to the non-linear device. Figure 5 shows the circuit configuration as induced in the above.

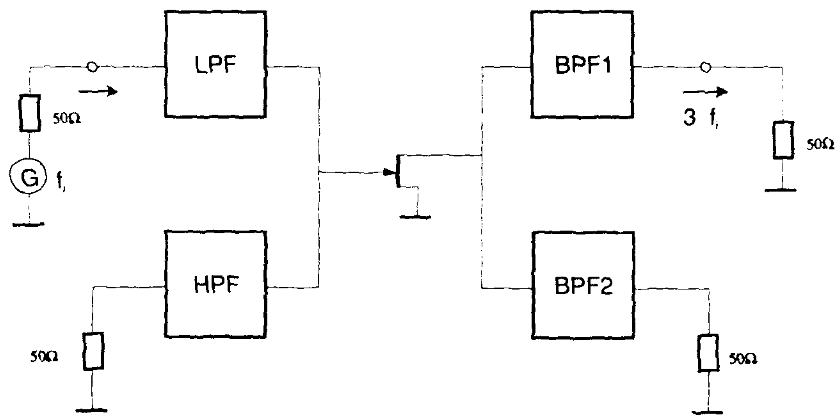

Fig. 5: Frequency tripler circuit topology featuring wide-band behaviour.

With respect to item 1), analysis of the circuit configuration yields the following:

- The generator's signal having fundamental frequency f_i passes the LPF and enters the gate,
- Harmonic components (except the fundamental frequency) leaving the gate pass the HPF and are absorbed in the dummy load,

- The third harmonic component having frequency 3 f_i leaving the drain passes BPF1 and constitutes the output signal,
- Other harmonic components leaving the drain pass BPF2 and are absorbed in the dummy load.

Since the LPF, HPF, and the BPF will be realized by means of approximately constant length transmission lines, the pass- and stop-bands will be mirrored and repeated around frequencies which are odd multiples of the $\lambda/4$-resonance frequency of the transmission lines. Hence, harmonic components with k= 9, 15 ,21, ... will pass BPF1 as if they were the wanted third harmonic component. Fortunately, the power levels associated with these harmonic components will be of no concern due to rapidly vanishing Fourier factors, lower MESFET gain[1)], and higher microstrip circuit losses.

It is noted that both the applied fundamental frequency and the extracted third harmonic component are of the odd type. Therefore, even the use of a balanced topology would not support separate or independant treatment of the two most important frequencies in a tripler-design and consequently is not adapted in frequency triplers.

Concludingly, item 1) is fulfilled except for some very high harmonic components.

With respect to item 2) analysis of the circuit configuration discloses the following:

- Harmonic components leaving the gate face the common junction of the input-diplexer, thus a 50 Ω resistance,
- Harmonic components leaving the drain face the common junction of the output-diplexer thus a 50 Ω resistance.

The 50 Ω resistance from the common junction is the result of an admittance compensation process. Exact diplexer synthesis technique exists so only inaccuracies in the (microstrip) implementation may lead to residual mismatch.

Concludingly, item 2) is fulfilled for all input frequencies and associated harmonic components.

A literature search has been performed and the resulting computer listing is available from the author. The number of articles treating the frequency tripler is clearly limited.

---

1) The effect of lower MESFET gain for higher frequencies on reduction of unwanted harmonic components depends on the location of the responsible non-linearity in the equivalent circuit.

One part deals with the frequency tripler in a highly theoretical/mathematical fashion but has been written to a large extent in Russian. Another part is of the practical/experimental type but deals with frequency triplers almost exclusively suited for sub-millimeter wavelengths (> 100 GHz), e.g. [9]. Only one article has been found about a microwave frequency tripler operating below 100 GHz ([10]).

The title of [9] suggests the described frequency tripler to have an operational band-width from 200 GHz to 290 GHz. This range turns out to be the tuneable band-width (requiring RF and bias optimization) rather than instantaneous band-width.

[10] describes a frequency tripler using a varactor diode and matching and filter circuits in microstrip. The reported measurements indicate -11 dB peak conversion efficiency at 0.2 W input power and a band-width of approximately 2%.

Concludingly:

- The number of articles treating the frequency tripler is clearly limited,
- No design techniques at all for or practical examples of frequency triplers with wide-band performance have been encountered in literature by the author.

The frequency tripler circuit topology as shown in figure 5 remains unmodified and is directly implemented into microstrip technology. A photograph of the implementation is shown in figure 6.

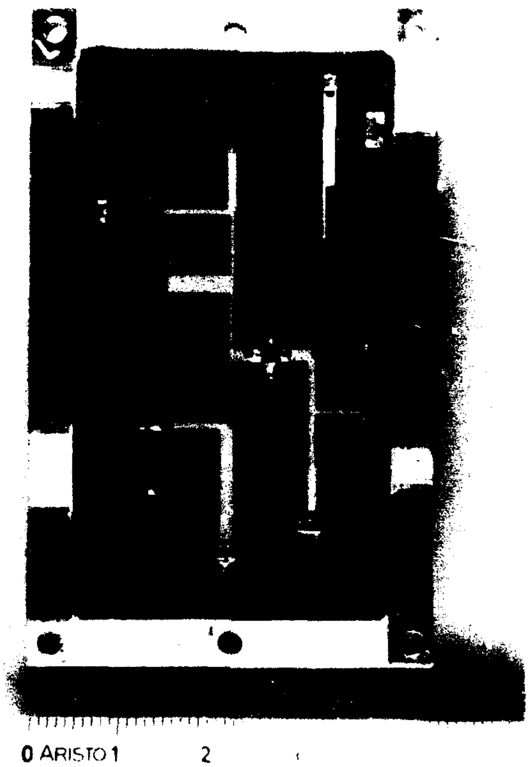

Fig. 6: Photograph of wide-band frequency tripler (S-band to X-band). The design is based on the concept of wave-form invariance to achieve wide-band performance.
The left-hand side of the small-signal MESFET in the centre is connected to the input-diplexer of which the lower branch is terminated by a 50 Ω dummy-load and the upper one forwards the input-signal.
The right-hand side of the MESFET is connected to the output-terminal through the upper branch of the output-diplexer.
Gate DC-voltage is applied by means of the resistively loaded and bended λ/4-stub in the left upper-corner. The drain DC-current is fed through the output-diplexer's lower branch 50 Ω dummy-load.

The $\lambda/4$-stub for gate bias is loaded by an 18 Ω-resistor for subdued impedance frequency sensitivity so that the admittance design goal is more or less met. The drain DC-supply does not alter present RF-impedances so that the admittance design goal remains entirely met.

Both the input-diplexer as well as the output-diplexer have been designed according to [2] and have been built first on separate substrates, each with three microstrip/SMA-adapters for experimental purposes. For each diplexer the reflection coefficient at the central node and the two transfer functions have been measured and are shown in appendices C and D. The mechanical (and hence electrical) contacts of the adapters from the output-diplexer were not optimal; this caused degradation of the reflection-coefficient and at the higher frequencies also of the S_{31}-transfer function.

3.2 Measurement results of a wide-band frequency tripler

The frequency tripler as described in paragraph 3.1 and shown in figure 6 has been subjected to measurement of conversion efficiency and strength of unwanted harmonic components at the output port.

The measurements have been performed using the same set-up as has been used for the frequency doubler.

The conversion efficiency is shown in appendix E: Frequency tripler conversion efficiency (note the 1 dB per division scale). It turns out to be (-10.4 ± 0.6) dB over the 8.5 ... 10.5 GHz design band at 10 dBm drive, 3 V input voltage (0.5 V drain voltage), and 30 mA drain current. Actually, a wider frequency response has been achieved but the prime focus was on the design band.

The absolute power levels of the first four harmonic components are shown in appendix F: Frequency tripler harmonic components. The suppression of unwanted harmonic components with respect to the third one ranges from -48 ... -14 dBc.

Concludingly, the current frequency tripler does exhibit the anticipated wide-band response and moderate spectral purity.

4 CONCLUSIONS AND RECOMMENDATIONS

Wave-form variance is an alternative and generic concept to achieve wide-band performance of microwave frequency multipliers. It is feasible to identify and formulate a practical design-goal: constant admittance at the terminals of the non-linear device within each harmonic sub-band.

An S-band frequency doubler has been designed and built a as first example of this approach. Measurement results indicate the frequency doubler does exhibit the anticipated wide-band response.

An X-band frequency tripler has been designed and built as a second example of this approach. Measurement results indicate the frequency tripler does exhibit the anticipated wide-band response.

Both examples prove the validity and practical suitability of this alternative concept.

It is recommended to monitor drain and gate voltages by means of a microwave sampling-oscilloscope for visualization of the wave-form invariance.

It is suggested that values other than 50 Ω as specific design-goal will be experimented with in order to potentially reduce power-loss due to general impedance mismatch at the ports of the MESFET.

It is recommended to improve wide-band behaviour of DC-feeding lines for the active device through resistive loading or replacement by an inductive coil with high resonance frequency.

Preceeding or succeeding system parts should show a 50 Ω match by themselves, otherwise an isolator or buffer-stage must be inserted.

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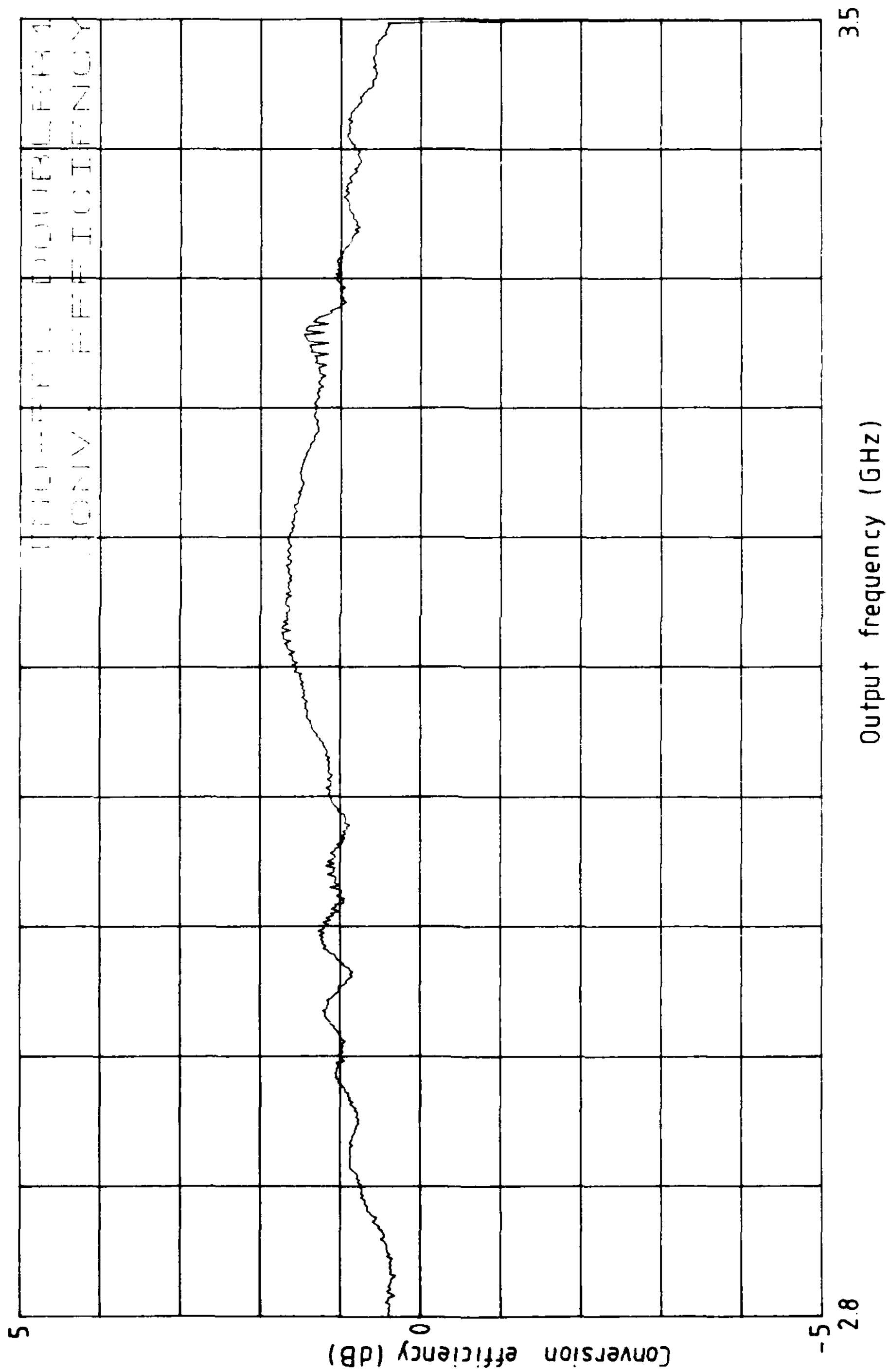
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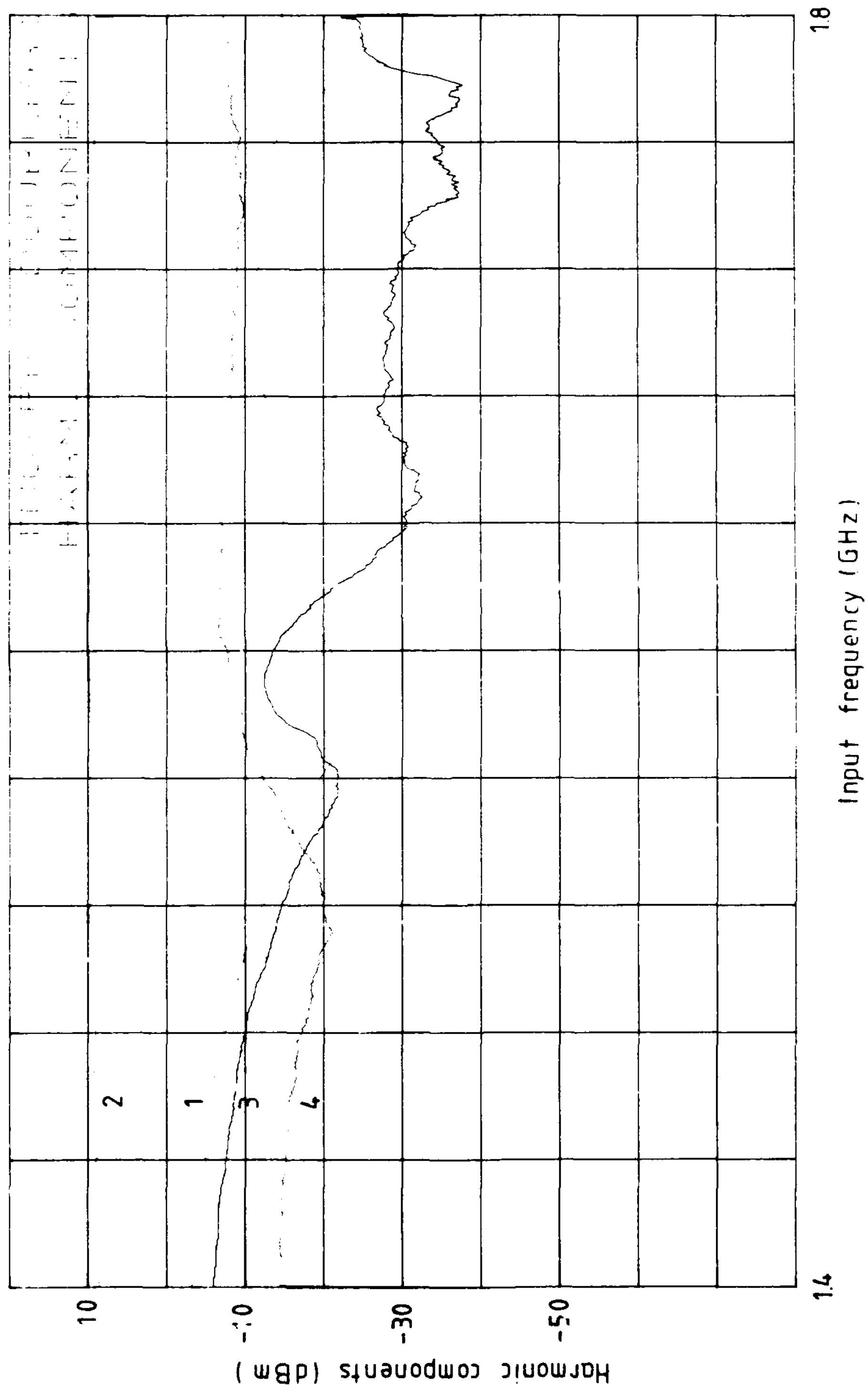
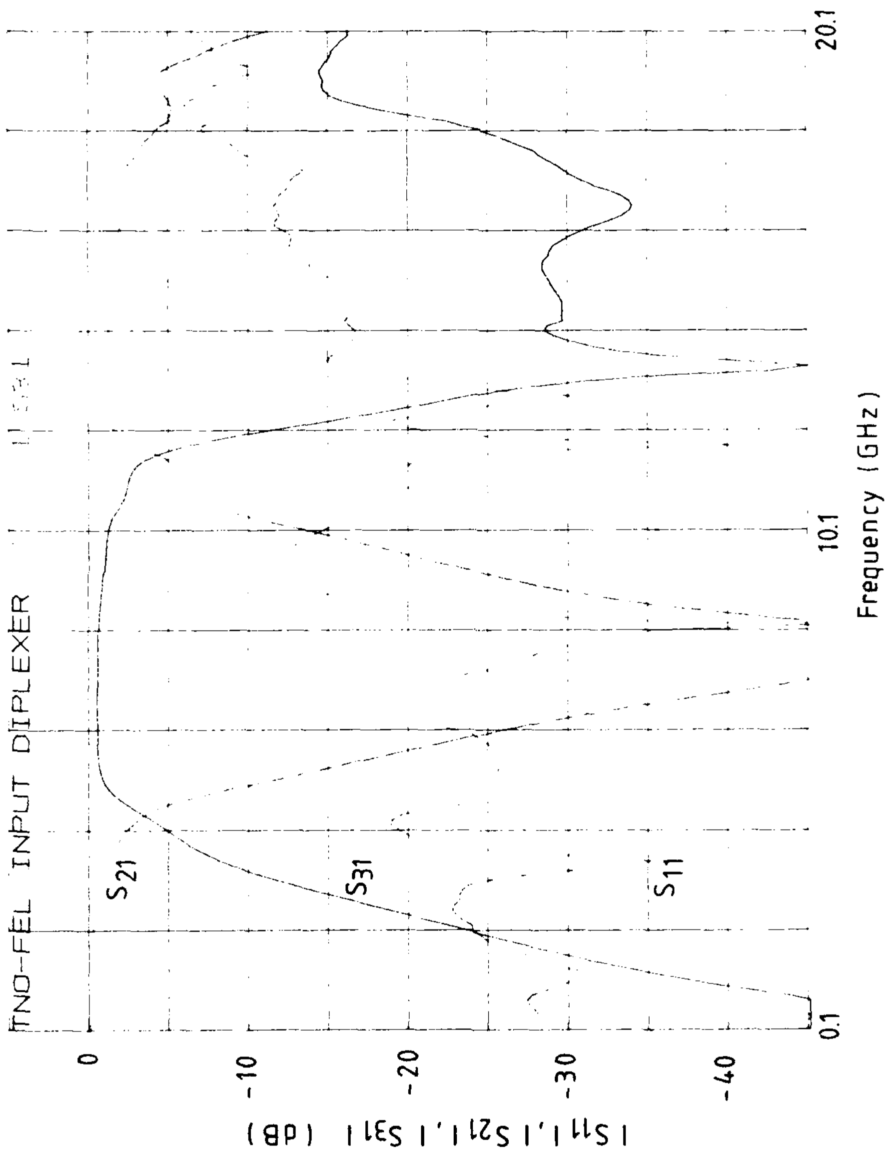
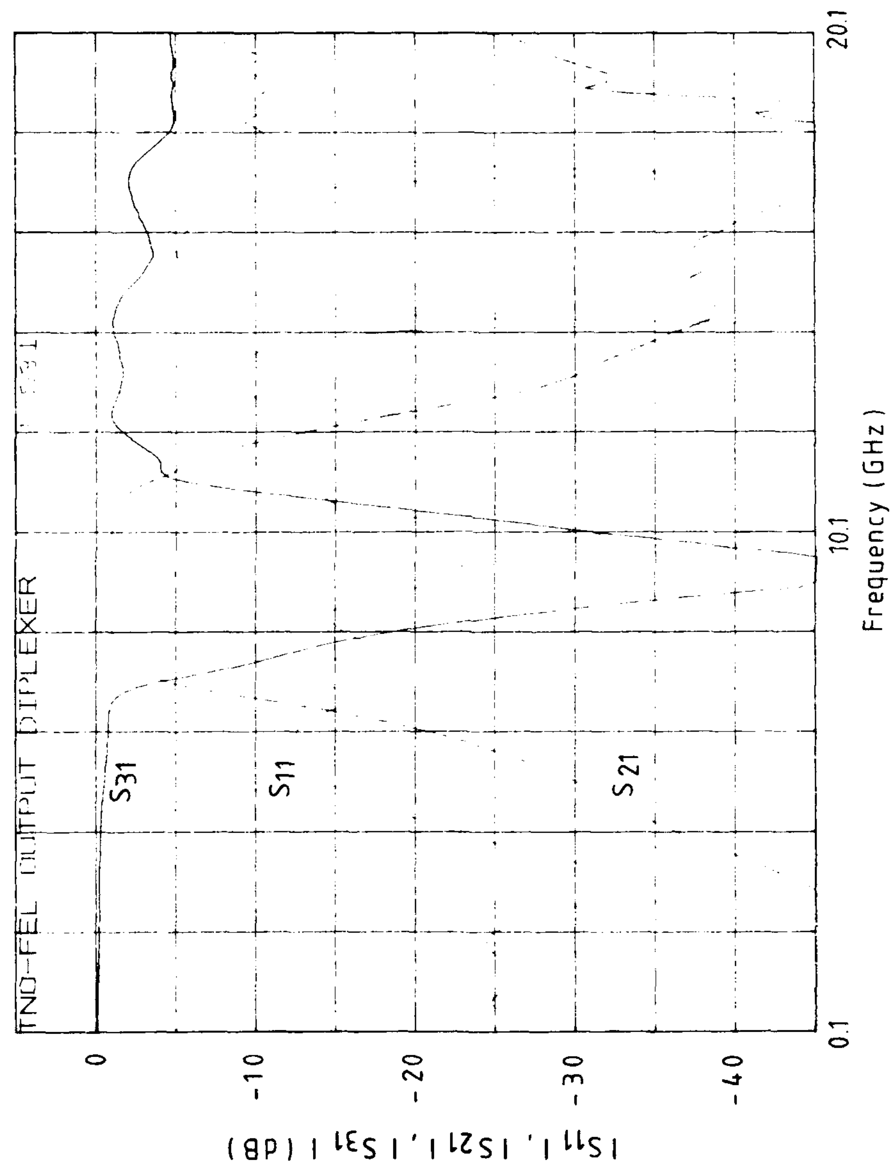
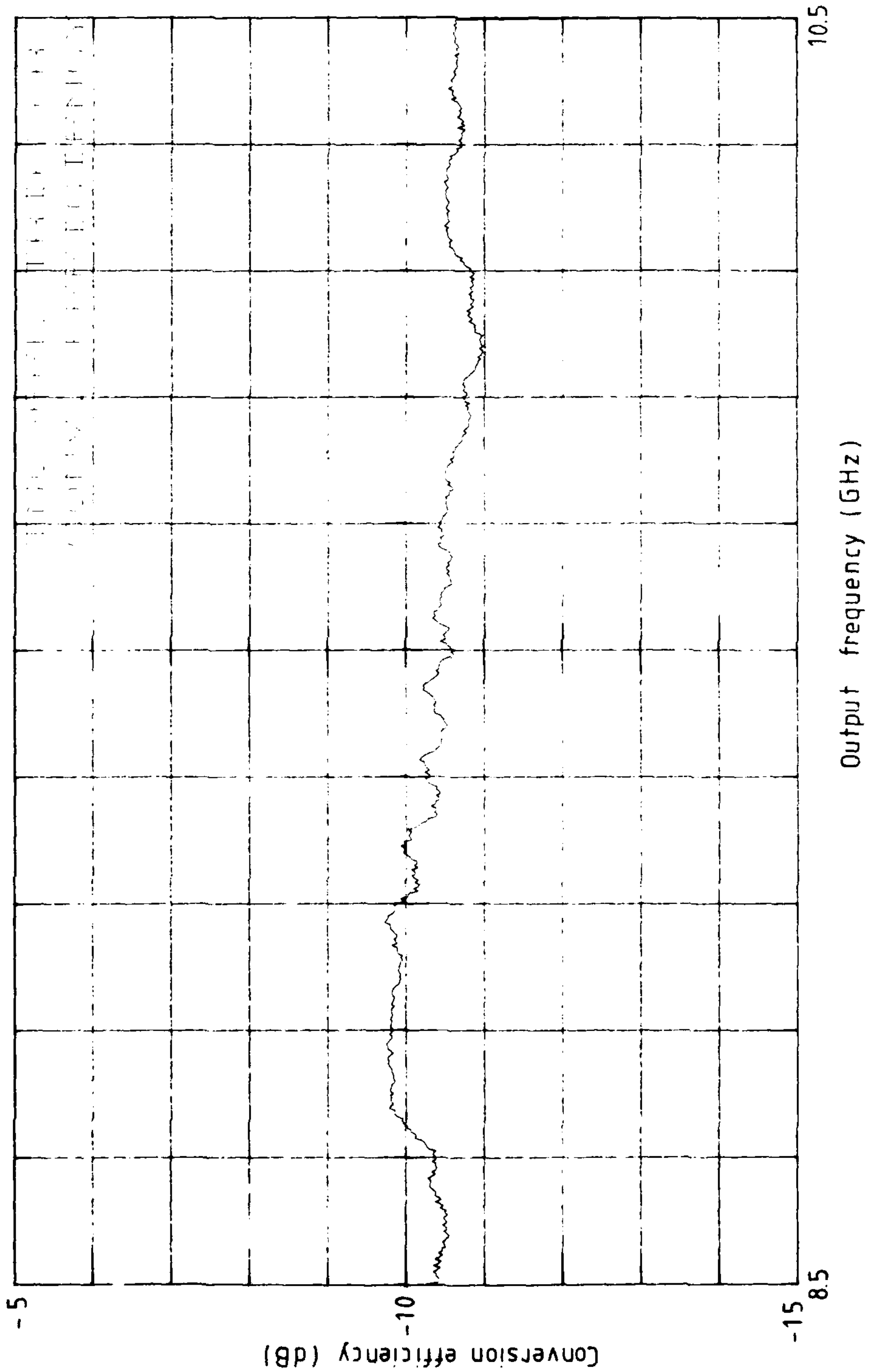
3.5
2.8
Conversion efficiency (dB)
5
0
-5

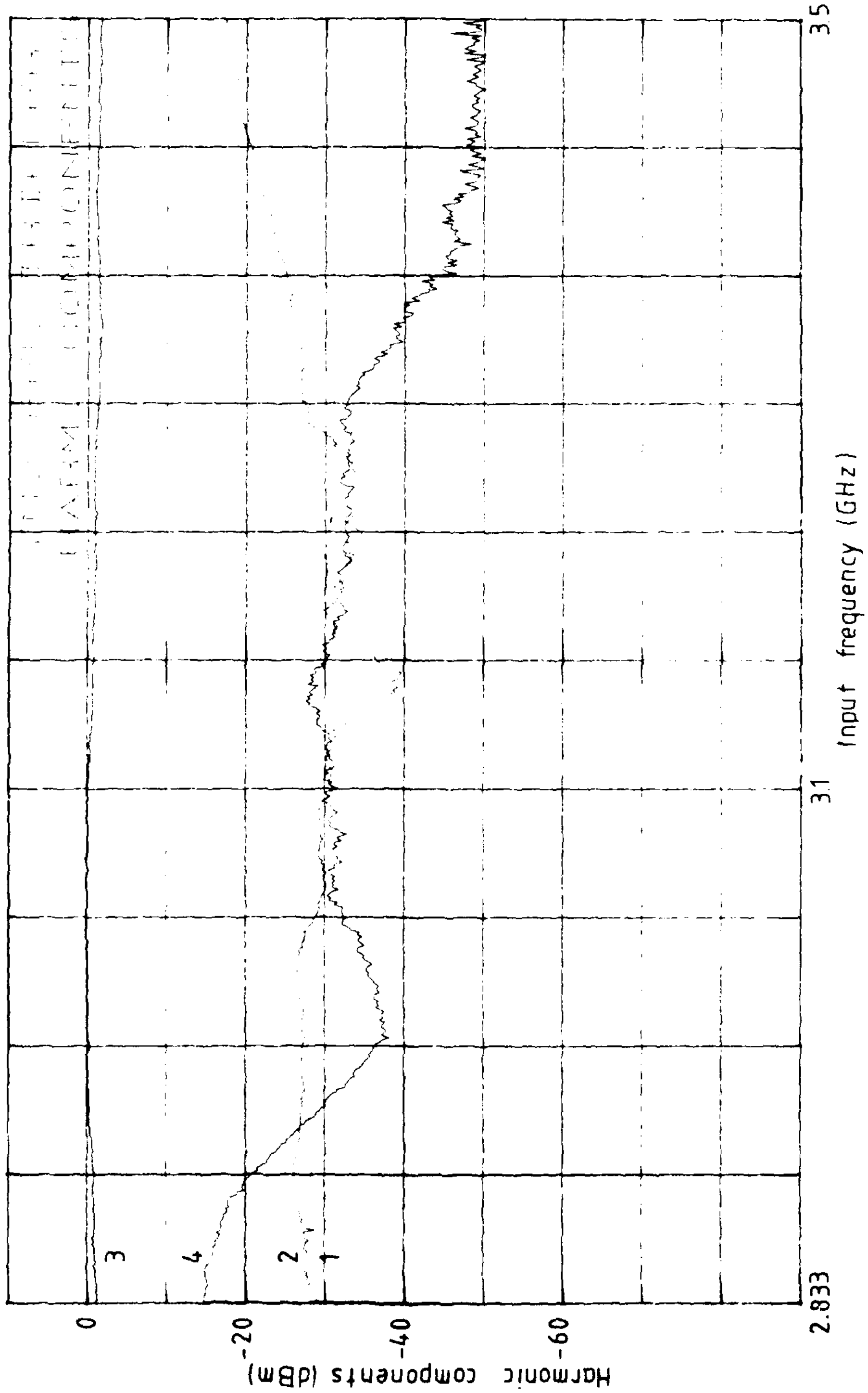

1.8
1.4
Input frequency (GHz)
10
-10
-30
-50
Harmonic components (dBm)
1
2
3
4


TNO-FEL INPUT DIPLEXER
S21
S31
S11
0
-10
-20
-30
-40
| S11 |,| S21 |,| S31 | (dB)
0.1
10.1
20.1
Frequency (GHz)


TNO-FEL OUTPUT DIPLEXER
S31
S11
S21
0.1
10.1
20.1
Frequency (GHz)
0
-10
-20
-30
-40
|S11|, |S21|, |S31| (dB)

Appendix E: Frequency tripler conversion efficiency




Harmonic components (dBm)
0
-20
-40
-60
Input frequency (GHz)
2.833
3.1
3.5
1
2
3
4

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DESIGN OF INHERENTLY WIDE-BAND MICROWAVE FREQUENCY DOUBLER AND TRIPLER IN MICROSTRIP

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TWO MODERN WIDE-BAND AND FREQUENCY AGILE RADAR SYSTEMS, CURRENTLY UNDER CONSTRUCTION AT TNO-FEL, REQUIRE THE DEVELOPMENT OF A WIDE-BAND S-BAND FREQUENCY DOUBLER AND A WIDE-BAND X-BAND FREQUENCY TRIPLER. THE WIDE-BAND REQUIREMENT, HOWEVER, IS HARD TO MEET WHEN USING THE CLASSICAL APPROACH. WAVE-FORM INVARIANCE AS AN ALTERNATIVE CONCEPT TO ACHIEVE INHERENTLY WIDE-BAND BEHAVIOUR IS PROPOSED. FROM THIS, A NEW DESIGN GOAL IS DERIVED AND FORMULATED: CONSTANT ADMITTANCE AT THE TERMINALS OF THE NON-LINEAR DEVICE WITHIN EACH HARMONIC SUB-BAND. A FREQUENCY DOUBLER HAS BEEN DESIGNED AND BUILT BASED ON THIS CONCEPT; THE CONVERSION EFFICIENCY MEASURES (1.0 ± 0.7) DB IN THE 2.8 ... 3.6 GHZ DESIGN BAND. ALSO, A FREQUENCY TRIPLER HAS BEEN DESIGNED AND BUILT BASED ON THIS CONCEPT; THE CONVERSION EFFICIENCY MEASURES (-10.4 ± 0.6) DB IN THE 8.5 ... 10.5 GHZ DESIGN BAND. BOTH EXAMPLES PROVE THE VALIDITY AND PRACTICAL SUITABILITY OF THIS ALTERNATIVE CONCEPT.

16. DESCRIPTORS	IDENTIFIERS
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X-BAND	FREQUENCY TRIPLER
DESIGN	WIDE-BAND
	MICROSTRIP
	WAVE-FORM INVARIANCE

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